MODELLING AND CONTROL OF ACTIVE CLAMPED FORWARD CONVERTER WITH SYNCHRONOUS RECTIFICATION

SUBODH MISHRA (111EE0140)

DEPARTMENT OF ELECTRICAL ENGINEERING

NATIONAL INSTRITIUTE OF TECHNOLOGY, ROURKELA

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MODELLING AND CONTROL OF ACTIVE CLAMPED FORWARD CONVERTER WITH SYNCHRONOUS RECTIFICATION

A thesis submitted in partial fulfillment of the requirements for the degree of

Bachelor of Technology in ELECTRICAL ENGINEERING

By

Subodh Mishra (111EE0140)

Under the guidance of

Prof. Susovon Samanta

DEPARTMENT OF ELECTRICAL ENGINEERING

NATIONAL INSTRITIUTE OF TECHNOLOGY, ROURKELA

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CERTIFICATE

This is to certify that the thesis titled "Modelling and control of Active Clamped Forward Converter with Synchronous Rectification", submitted to the National Institute of Technology, Rourkela by **Mr. Subodh Mishra**, bearing Roll No. **111EE0140**, for the award of the degree **Bachelor of Technology in Electrical Engineering,** is a genuine record of research work carried out by him under my supervision during the session 2014-2015.

The thesis is based on candidate's own work and has not been submitted elsewhere for a degree/diploma.

In my opinion, the thesis is of the standard required for the award of a **Bachelor of Technology in Electrical Engineering.**

Professor Susovon Samanta

Supervisor

Department of Electrical Engineering

National Institute of Technology-Rourkela

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111EE0140

Table of Contents

Certificate 2

Acknowledgements 3

List of figures 5

List of tables 6

Abstract 7

Chapter 1: Introduction 8

1.1: Advantages of using Active Clamping 9

1.2: High Side vs Low Side Clamping 9

1.3: The clamp capacitor 12

Chapter 2: Small Signal Modelling of Active Clamped Forward Converter 15

2.1: State Space Averaging of the Active Clamp Forward Converter 15

2.2: Derivation of the Transfer Function 19

2.3: Results 21

Chapter 3: Controller Design 22

3.1: Controller Design 22

3.2: Results 23

Chapter 4: Conclusions and Future work 29

References: 30

List of Figures

1. Low side clamp circuit.

2. MOSFET Drain to Source voltage vs input voltage for varying N and fixed output voltage.

3. High Side Clamp Circuit.

4. Bode plot of uncompensated system.

5. Block diagram of a DC Regulator with control elements.

6. Bode plot of compensated system.

7. Simulink Transfer function based block diagram of compensated system.

8. Output voltage vs time (both lead and lag compensators used).

9. Output voltage vs time (with lag (PI) compensator removed).

10. Closed loop Circuit schematic in Simulink Environment.

11. Voltage waveform of the compensated circuit.

12. Current waveform of the compensated circuit.

13. Voltage waveform of the circuit with only lead compensator.

14. Current waveform of the circuit with only lead compensator

List of Tables

1. Comparison of Active Clamping vs RCD Clamping.

2. Comparing High side and Low side clamping.

ABSTRACT

This work presents the study of an active clamped forward converter with synchronous rectifiers. The advantages of active clam circuit over RCD clamping has been discussed. The disadvantages of the active clamp circuit is also enlisted. The method for choosing a clamp capacitor is given. A comparative study between high side and low side clamping has been done. The small signal modelling of the active clamp circuit has been done and a transfer function has been derived. Using this transfer function a PID controller has been designed and its efficacy has been checked in SIMULINK. The difference in the output of the system and the increase in the steady state error when the PI compensator is not used is also seen, hence proving the necessity to include a PI controller along with a lag controller in the feedback path.

Chapter 1

INTRODUCTION

Forward converter topology is finding increasing applications where high currents with low voltages (e.g. telemetry applications) are needed without decreasing the circuit efficiency [1]. There are a number of techniques which can be used to reset the transformer used in this circuit but active clamp transformer reset circuit has proved to give significant performance enhancements. The active clamp forward converter has an auxiliary switch along with a capacitor which helps in resetting the transformer [2]. The clamp capacitor conducts when the main switch is off and it supplies the energy required during each cycle with negligible amount of losses. A large value of clamp capacitance keeps the associated voltage ripple to a minimum. The conventional RCD clamping methodology can be used to decrease the energy stored in leakage inductance, thus reducing the voltage stress on the switch. But there is no significant improvement in the overall converter efficiency [3]. The surge energy stored in leakage inductance is transferred to the active clamp capacitor thereby decreasing the voltage stress on the main switch [4].

The major differences between active clamping and RCD clamping can be given as follows:

Table 1. Comparison of Active Clamping vs RCD Clamping

Active Clamping	RCD Clamping
Major portion of leakage energy is recovered	Major portion of leakage energy is lost in the form of heat
ZVS Reduces switching losses	Hard Switching increases losses
No issue of electromagnetic induction due to absence of spikes in voltages across main switch.	Due to hard switching, electromagnetic induction can occur.
Implementation of synchronous rectification is easier	Implementation of synchronous rectification is difficult
Energy Stored in leakage inductance can be recovered in a lossless manner by clamp capacitor	

1.1 Advantages of using Active Clamping

The advantages of active clamp/reset techniques can be summarized as follows:

- No reset winding and dissipative clamps are required
- Higher maximum duty cycle possible
- The energy stored in parasitic elements is transferred to tank elements and recycled, resulting in higher efficiency and lower noise.
- Zero Voltage Switching (ZVS) of switched is possible and this giver higher efficiency.
- The transformer waveform allows easy implementation of synchronous switching scheme on the secondary side.
- Reduced Electromagnetic Interference.

The few disadvantages associated with this circuit are:

- A precise duty cycle clamping is necessary. If the duty cycle is not clamped to some maximum value, then increased duty cycle can saturate the transformer core which results in additional voltage stress on the main switch [5].
- An improved and robust control technique is required to adjust the delay between switching of main switch and the auxiliary switch.

1.2 High Side vs Low Side Clamping

In the high side clamping the clamp circuit is connected across the primary winding of the transformer and in the low side clamping the clamp circuit is connected across the main MOSFET switch.

a. Low Side Clamp Circuit

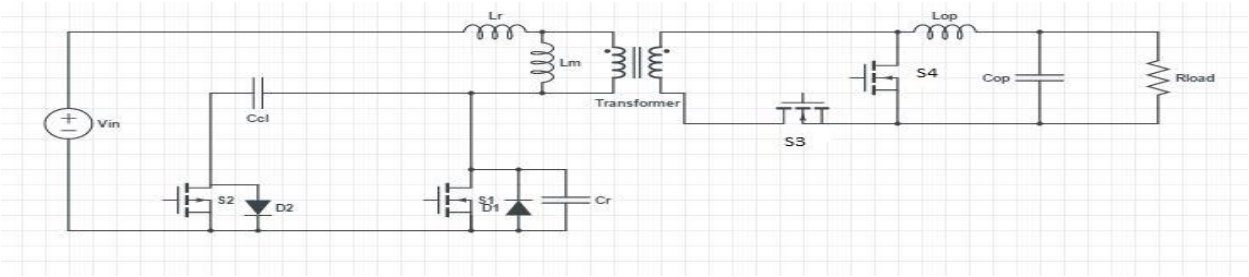

Fig 1. Low side clamp circuit.

When S1 conducts the input voltage appears across the transformer primary. When S2 conducts the difference between the clamp capacitance voltage and the input voltage appears across the transformer primary. It should be kept in mind that the magnetizing current only flows through S2. When S2 conducts, the transformer resets.

At times when neither of the switches are conducting, the body diodes conduct. The conduction of the body diodes is a prerequisite for ensuring Zero Voltage Switching (ZVS).

The voltage across the clamp capacitor can be found by volt second balance and found to be:

$$V_{c(LS)} = \frac{1}{1-D} V_{IN} \quad (1.1)$$

D = duty cycle; V_{IN} = Input Voltage

During the transformer reset period the dot polarity reverses so the voltage applied across the transformer becomes:

$$V_{Reset} = V_{C(LS)} - V_{IN} \quad (1.2)$$

The above equation can be simplified using the value for $V_{C(LS)}$ and the final result will be:

$$V_{Reset(LS)} = \frac{D}{1-D} V_{IN} \quad (1.3)$$

$$now, D = \frac{V_o}{V_{in}} N \quad (1.4)$$

$$using\ these\ equations, V_{Reset(LS)} = \frac{V_o * V_{in} * N}{V_{in} - N V_o} \quad (1.5)$$

$$and, V_{DS(LS)} = V_{C(LS)} = \frac{V_{IN}^2}{V_{IN} - N * V_o} \quad (1.6)$$

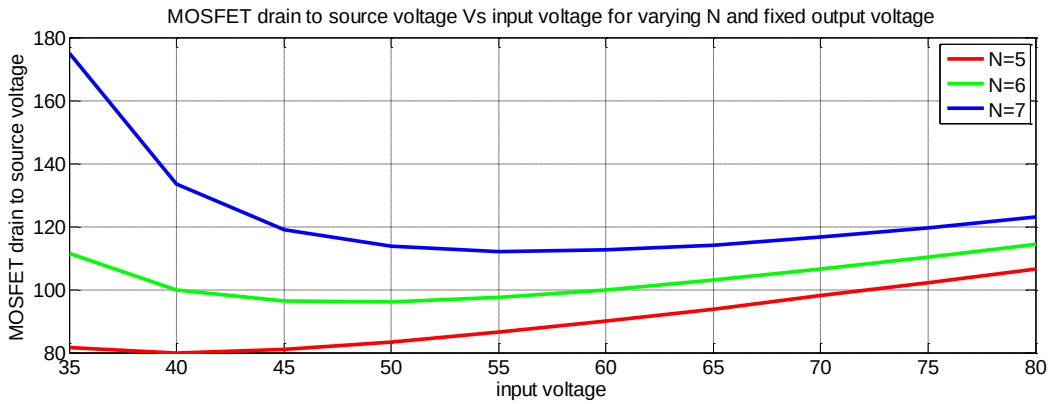

Fig2.

From the above figure we see a substantial difference in drain to source MOSFET voltage stress when the minimum input voltage is applied. This implies that the PWM control must accurately limit the maximum duty cycle. If that is not done then the voltage stress across the MOSFET could be disastrously high. From the graph we can see that for a standard forward converter functioning with the full telecom voltage range (36<V<75) as input, a turns ratio of N=6 results in V_{DS} = 110 V at V_{in}=36 V and 75 V [5]. Also the clamp capacitor must be carefully selected.

b. High side Clamp

Refer to the figure below. When the main MOSFET S1 conducts the input voltage appears across the primary winding and when the auxiliary MOSFET S2 is conducting the clamp voltage appears across the transformer. Just as it occurred in the case of Low Side Clamp, the transformer reset occurs when S2 conducts. This is different from low side case where the clamp capacitor voltage was applied directly across the main MOSFET. Like the main switch, the auxiliary MOSFET is also N channel.

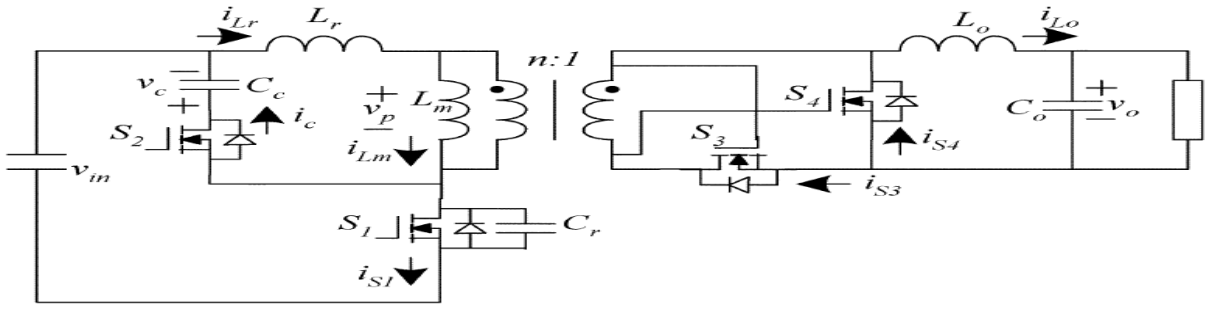

Fig 3. High side clamp circuit

By volt second balance, we obtain the following equation for voltage across the clamp capacitor:

$$V_{C(HS)} = \frac{D}{1-D} V_{in} \quad (1.7)$$

$$V_{Reset(HS)} = V_{C(HS)} = \frac{D}{1-D} V_{in} \quad (1.8)$$

As the voltage polarity across the transformer primary becomes opposite during reset period, the voltage applied to drain to source of the main MOSFET S1 can be written as

$$V_{DS(HS)} = V_{IN} + V_{C(HS)} \quad (1.9)$$

On using the above equations we get:

$$V_{DS(HS)} = \frac{V_{IN}}{1-D} \quad (1.10)$$

Using the value of D as used in previous case we obtain the following:

$$V_{DS(HS)} = \frac{V_{IN}^2}{V_{IN} - NV_o} \quad (1.11)$$

From the above equation we can clearly see that: $V_{DS(HS)} = V_{DS(LS)}$ (1.12)

1.3 The clamp capacitor:

High side or low side clamping; the volt second balancing condition is mandatory for each case. As the switch S1's drain to source voltage and transformer reset are the same for both of the circuits it's the difference in the clamp voltages across the clamp capacitor that must be

considered while choosing either of the two configurations.

If we compare the difference between the clamp voltages for each case, we have

$$\Delta V = V_{C(LS)} - V_{c(HS)} \quad (1.13)$$

Replacing $V_{C(LS)}$ and $V_{C(HS)}$ with expressions derived earlier, we get:

$$\Delta V = V_{in} \quad (1.14)$$

We can see, $V_{C\,(LS)}$ is more than $V_{C(HS)}$ by V_{in}.

The maximum allowable ripple voltage helps determining the value of clamp capacitor's capacitance. High values of capacitance result in less ripple voltage but may also result in transients that will take a while to settle down or may never settle down. In general, the clamp capacitor is permitted to have some ripple but not enough to add excessive drain to source voltage stress to main switch S1. Ideally 20% ripple is allowed

The following condition if used during determination of clamp capacitor value, the resonant time constant must be much greater than the maximum off time [5]. If put in an inequality, it will be given as:

$$2\pi\sqrt{L_{mag} \times C_{CL}} > 10 \times t_{off(max)} \quad (1.15)$$

$$on\ simplifying\ the\ above\ equation\ we\ get, C_{CL} > \frac{10((1 - D_{\min}))^2}{(2\pi F_{SW})^2 \times (L_{mag})} \quad (1.16)$$

Table 2. Comparing High side and Low side clamping

	High Side Clamp	Low Side Clamp
V_{DS}	$\frac{V_{IN}}{1-D}$	$\frac{V_{IN}}{1-D}$
V_{RESET}	$\frac{D}{1-D}V_{in}$	$\frac{D}{1-D}V_{in}$
V_C	$\frac{D}{1-D}V_{in}$	$\frac{1}{1-D}V_{in}$
$C_{Cl}(on\ basis\ of\ the\ clamp\ capacitor\ voltage)$	Voltage lesser by V_{IN} Volts Highest value of clamp capacitor voltage occurs at	Voltage greater by V_{IN} Volts Transformer turns limits the clamp capacitor voltage

	maximum duty cycle. Care must be taken during wide range V_{IN} applications	Care must be taken during off line high voltage applications
$C_{Cl}(component\ value)$	Similar for both cases	Similar for both cases
AUXILIARY-MOSFET	N-Channel	P-Channel

In case of low side clamping we get a slight higher, yet better controlled clamp voltage provided the turn ratio of the transformer is properly selected as per the figure 2.

Chapter 2

SMALL SIGNAL MODELLING OF ACTIVE CLAMPED FORWARD CONVERTER

Before Small Signal Modelling, the State Space modelling of the system is done. State space modelling is one of the most widely used techniques in the modeling and control of DC-DC power converters. In the state space model of the active clamped forward converter that we develop here, the circuit parasitics are all neglected to make calculations and derivation of transfer function easier. The biggest assumption made here is that the forward converter is functioning in the continuous current mode. The circuit operation is divided into two modes, one in which the main switch is on and the auxiliary switch is off and the other in which the auxiliary switch is on and the main switch is off. Differential equations governing each of the modes are written and are finally combined together using the popular state space averaging technique. This technique can be used to derive the transfer function of the system. The knowledge of the system transfer function will aid in the design of compensators required to meet the performance criteria. The biggest advantage of state space averaging method is the generality of the result obtained.

2.1 State Space Averaging of the Active Clamp Forward Converter

Proceeding with the state space modelling

1. Mode 1: 0<t<DT: (on condition)

   Here D= duty cycle

   T= Time period=$\frac{1}{\text{Switching Frequency}(F_{SW})}$

   The state variables are output capacitor voltage, output inductor current, clamp capacitor voltage, magnetizing inductance current, respectively.

   vC=output capacitor voltage, iL=output inductor current, vCC=clamp capacitor voltage, iM=magnetizing current, C=output capacitance, R=Load resistance, Rc=parasitic resistance of output capacitor, L=output inductor, RL=parasitic resistance of output inductor, Lm=magnetizing inductance, Rcc=Parasitic resistance of clamp capacitor, vg=input voltage, Cc=clamp capacitance, N=turns ratio

$$\begin{bmatrix} dvC/dt \\ diL/dt \\ dvCC/dt \\ diM/dt \end{bmatrix} = \begin{bmatrix} -1/C(R+Rc) & R/C(R+Rc) & 0 & 0 \\ -R/L(R+Rc) & -(RL/L+RRc/L(R+Rc)) & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} vC \\ iL \\ vCC \\ iM \end{bmatrix} + \begin{bmatrix} 0 \\ 1/NL \\ 0 \\ 1/Lm \end{bmatrix} \text{vg}$$

(2.1)

$$\text{Vout} = \begin{bmatrix} R/(R+Rc) & R/C(R+Rc) & 0 & 0 \end{bmatrix} \begin{bmatrix} vC \\ iL \\ vCC \\ iM \end{bmatrix} \qquad (2.2)$$

2. Mode 2: DT<t<T: (off condition)

$$\begin{bmatrix} dvC/dt \\ diL/dt \\ dvCC/dt \\ diM/dt \end{bmatrix} = \begin{bmatrix} -1/C(R+Rc) & R/C(R+Rc) & 0 & 0 \\ -R/L(R+Rc) & -(RL/L+RRc/L(R+Rc)) & 0 & 0 \\ 0 & 0 & 0 & 1/Cc \\ 0 & 0 & -1/Lm & -Rcc/Lm \end{bmatrix} \begin{bmatrix} vC \\ iL \\ vCC \\ iM \end{bmatrix} +$$

$$\begin{bmatrix} 0 \\ 0 \\ 0 \\ 1/Lm \end{bmatrix} \text{vg} \qquad (2.3)$$

$$\text{Vout} = \begin{bmatrix} R/(R+Rc) & R/C(R+Rc) & 0 & 0 \end{bmatrix} \begin{bmatrix} vC \\ iL \\ vCC \\ iM \end{bmatrix} \qquad (2.4)$$

By state space averaging we have: $A=DA_{on}+(1-D)A_{off}$

$$B=DB_{on}+(1-D)B_{off}$$

$$C=DC_{on}+(1-D)C_{off}$$

Using the above equations we get:

$$A=\begin{bmatrix} -1/C(R+Rc) & R/C(R+Rc) & 0 & 0 \\ -R/L(R+Rc) & -(RL/L+RRc/L(R+Rc)) & 0 & 0 \\ 0 & 0 & 0 & (1-D)/Cc \\ 0 & 0 & -(1-D)/Lm & -Rcc(1-D)/Lm \end{bmatrix} \quad (2.5)$$

$$B=\begin{bmatrix} 0 \\ D/NL \\ 0 \\ 1/Lm \end{bmatrix}, \quad C=\begin{bmatrix} R/(R+Rc) & R/C(R+Rc) & 0 & 0 \end{bmatrix} \quad (2.6)$$

By small signal modelling we have:

$$\dot{x}=Ax+Bu+((A_{on}-A_{off})X+(B_{on}-B_{off})U)d$$

Here X=steady state value of state variables

U=steady state value of input=Vg

x=small signal state matrix

d=small signal duty ratio

On substituting and simplifying the above equation we obtain the small signal modelling of the active clamped forward converter. This small signal model is given by:

$$\dot{x}=\begin{bmatrix} -1/C(R+Rc) & R/C(R+Rc) & 0 & 0 \\ -R/L(R+Rc) & -(RL/L+RRc/L(R+Rc)) & 0 & 0 \\ 0 & 0 & 0 & (1-D)/Cc \\ 0 & 0 & -(1-D)/Lm & -Rcc(1-D)/Lm \end{bmatrix} x+$$

$$\begin{bmatrix} 0 & 0 \\ D/NL & Vg/NL \\ 0 & -\mathrm{Im}/Cc \\ 1/Lm & (Vcc+Rcc\,\mathrm{Im})/Lm \end{bmatrix} \begin{bmatrix} vg \\ d \end{bmatrix} \quad (2.7)$$

$$y=vout=\begin{bmatrix} R/(R+Rc) & R/C(R+Rc) & 0 & 0 \end{bmatrix} x$$

This is the small signal state space model of the system model

To ease the calculations involved we neglect the circuit parasitics. This completely simplifies the matrices A, B and C in the small signal model.

For the model with no parasitics:

$$A=\begin{bmatrix} -1/CR & 1/C & 0 & 0 \\ -1/L & 0 & 0 & 0 \\ 0 & 0 & 0 & (1-D)/Cc \\ 0 & 0 & -(1-D)/Lm & 0 \end{bmatrix},$$

$$B=\begin{bmatrix} 0 & 0 \\ D/NL & Vg/NL \\ 0 & -\mathrm{Im}/Cc \\ 1/Lm & Vcc/Lm \end{bmatrix},$$

$$C=\begin{bmatrix} 1 & 0 & 0 & 0 \end{bmatrix}$$

Here, Vg, Im and Vcc are the steady state values of the input voltage, magnetizing current and clamp capacitor voltage respectively.

So, the steps involved in small signal modelling are:

1. Obtain the state space model for on mode or mode 1.
2. Obtain the state space model for off mode or mode 2.
3. Find the state averaged model by combining the models of mode 1 and mode 2.

4. Find the steady state values of all the state variables by setting their derivatives to zero in the state averaged model.
5. Obtain the small signal model.
6. Use the steady state values obtained in step 4 in the small signal model

The small signal model is now ready.

2.2 Derivation of the Transfer Function

Using the small signal model derived in the last section, the transfer function of the system can be obtained. As there are two different inputs, we will be having two different transfer functions. One will be the ratio of laplace transforms of output voltage to input voltage (when change in duty cycle is negligible) and another is the ratio of laplace transforms of output voltage to input duty cycle (when change in input voltage is negligible). The first one is called the line to output transfer function and the second one is called the control to output transfer function.

Line to output transfer function: $G_{vg}(s) = \frac{v(s)}{v_g(s)}, d(s) = 0$ (2.8)

Control to output transfer function: $G_{vd}(s) = \frac{v(s)}{d(s)}, v_g(s) = 0$ (2.9)

$G_{vd}(s)$ is the actual plant model which takes the control input and gives the output voltage, this transfer function appears in the loop gain, hence has a significant effect on the converter performance.

The converter transfer function can be derived from its small signal model. The method is as follows:

In small signal modelling as well as in state space model we have:

$\dot{x}(t)=Ax(t)+Bu(t)$

$y(t)=Cx(t)$

by taking the laplace transform of the above two equations we get:

$sX(s)=AX(s)+BU(s) \Rightarrow X(s)=(sI-A)^{-1}BU(s)$

$Y(s)=CX(s) \Rightarrow Y(s)=C(sI-A)^{-1}BU(s) \Rightarrow Y(s)/U(s)= C(sI-A)^{-1}B$ (2.10)

Using the above method we can determine the transfer function of the converter from its small signal state space model.

Owing to the sparsity of the matrix A, the transfer function can be calculated by hand calculations, but to ensure correct and accurate results, the MATLAB symbolic math functions were used to obtain the transfer function.

MATLAB code snippet for obtaining transfer function:

```
clc;

clear;
%STEADY STATE ANALYSIS
syms R L C Lm Cc D N Vg s;
A=[-1/(R*C) 1/C 0 0;-1/L 0 0 0;0 0 0 (1-D)/Cc;0 0 -(1-D)/Lm 0]
B=[0;D/(N*L);0;1/Lm]
C=1*eye(4)
disp('Steady State Analysis');
Vo=-C(1,:)*inv(A)*B*Vg
IL=-C(2,:)*inv(A)*B*Vg
VCc=-C(3,:)*inv(A)*B*Vg
Im=-C(4,:)*inv(A)*B*Vg
%SMALL SIGNAL ANALYSIS
disp('Small Signal Analysis');
b=[B,[0;Vg/(N*L);-Im/Cc;VCc/Lm]];
trf=C(1,:)*inv((s*eye(4)-A))*b
```

Since we have two inputs, we will be having two transfer functions and they are:

$$G_{vg}(s) = \frac{v(s)}{v_g(s)} = \frac{DR}{N(RLCs^2 + Ls + R)} \quad (2.11)$$

$$G_{vd}(s) = \frac{v(s)}{d(s)} = \frac{RV_g}{N(RLCs^2 + Ls + R)} \quad (2.12)$$

Symbols have their usual meaning.

In our model

R=0.1 ohm; L=4.67e-6 H; C=2306.2e-6 F; Lm=65.05e-6 H; Cc=191e-9 F; D=0.5; N=6; Vg=48 V;

Substituting these values in the equations above:

$$G_{vg}(s) = \frac{v(s)}{v_g(s)} = \frac{7.7376 \times 10^6}{(s^2 + 4336s + 9.285 \times 10^7)} \quad (2.13)$$

$$G_{vd}(s) = \frac{v(s)}{d(s)} = \frac{7.4281 \times 10^8}{(s^2 + 4336s + 9.285 \times 10^7)} \quad (2.14)$$

2.3 Results

The examination of the bode plot of the control input to output transfer function derived in the last section shows that the phase margin of the system is 9.65 degree at 4.567 kHz.

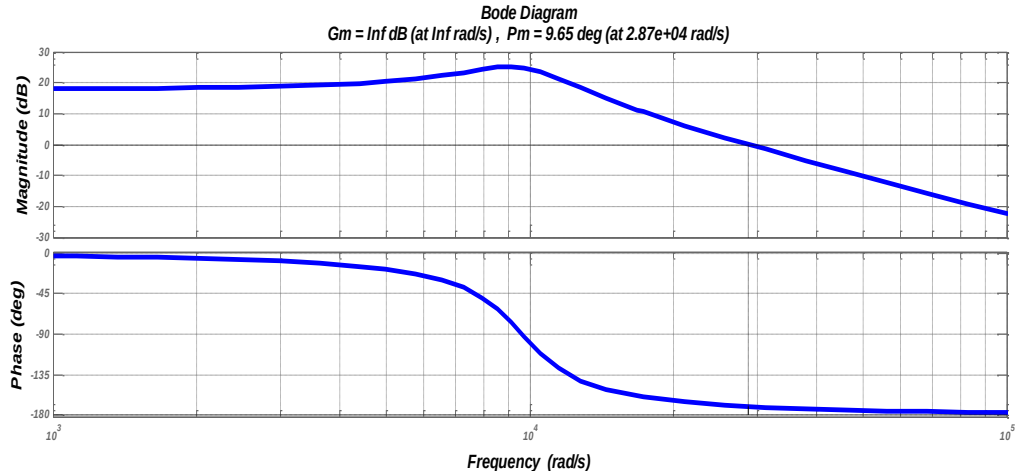

Fig 4: Bode plot of uncompensated system

According to control theory of converters the phase margin should be between 50 to 60 degrees for enhanced stability of the system (7). Keeping this point in mind, a controller has been designed. The design specification is: a cutoff frequency of 10 kHz (one 10^{th} of the switching frequency) and a phase margin of 55 degree. To meet these specifications, the compensator must make the overall magnitude of loop gain equal to unity at 10 kHz besides improving the phase margin. This issue has been addressed in the next chapter.

Chapter 3

CONTROLLER DESIGN

A simple voltage mode controller has been designed for the active clamp forward converter circuit. The controller has been verified by running SIMULINK Simulations.

The block diagram of a converter system with controller is given as follows:

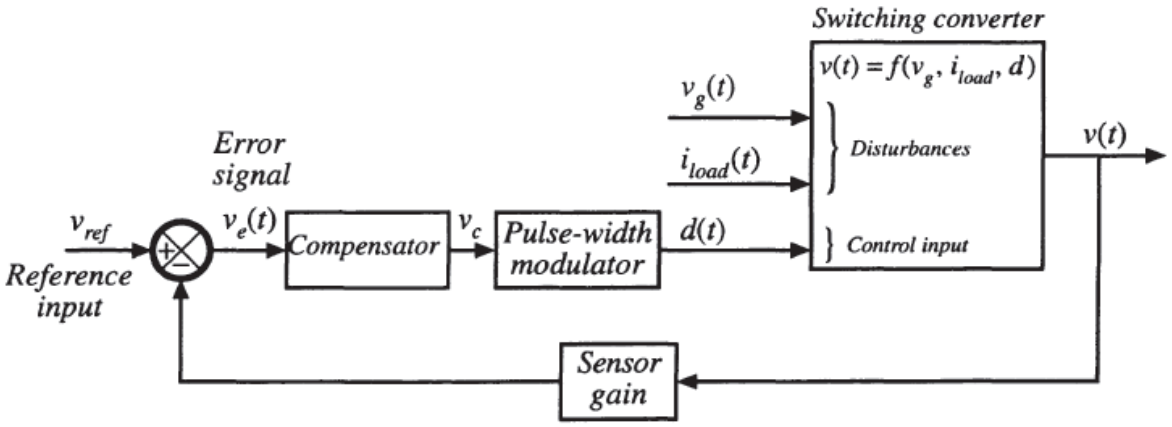

Fig 5: Block diagram of a DC Regulator with control elements

3.1 Controller Design

Like discussed in the last chapter phase margin should be between 50 to 60 degrees and the design specification is 55 degree of phase margin at a cutoff frequency of 10 kHz

To improve the DC gain of the system an inverted zero compensator is also introduced in the loop, thus making the overall compensator a PID controller.

Now:

$$f_z = 10000\sqrt{\frac{1-\sin 55}{1+\sin 55}} = 3152.98\,Hz \quad (3.1)$$

$$f_p = 10000\sqrt{\frac{1-\sin 55}{1+\sin 55}} = 31715.95\,Hz \quad (3.2)$$

The dc gain of the compensator was also calculated and found to be: $G_{c0} = 6.562$

The inverted zero compensator was also determined by placing it at a frequency equal to 1/20 th of the switching frequency ie. at 500 Hz. The inverted zero compensator (Lag compensator) together with the lead compensator make up a PID controller. The lag compensator improves the phase margin thus enhancing the system stability and the lead compensator improves the DC gain there by reducing the steady state error.

The overall compensator transfer function equals:

$$G_{c0} = 6.562\left(1+\frac{2\pi\times 500}{s}\right)\left(\frac{1+5.04776\times 10^{-5}s}{1+5.01814\times 10^{-6}s}\right) \quad (3.3)$$

Using this compensator significantly improves the phase margin and also improves the DC gain.

3.2 Results

The bode plot of the system with compensator in loop is given next:

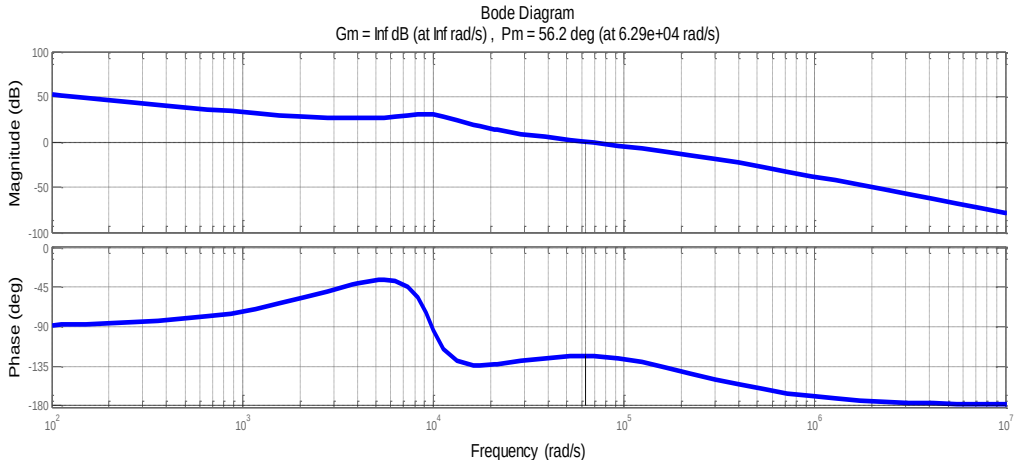

Fig 6: The bode plot of the compensated system

The new phase margin is found to be 56.2 degree at 10010.84 Hz. Thus we see that the design specifications are met.

Verification of the controller efficacy in Simulink:

a. Verification by block Simulink transfer function block diagrams

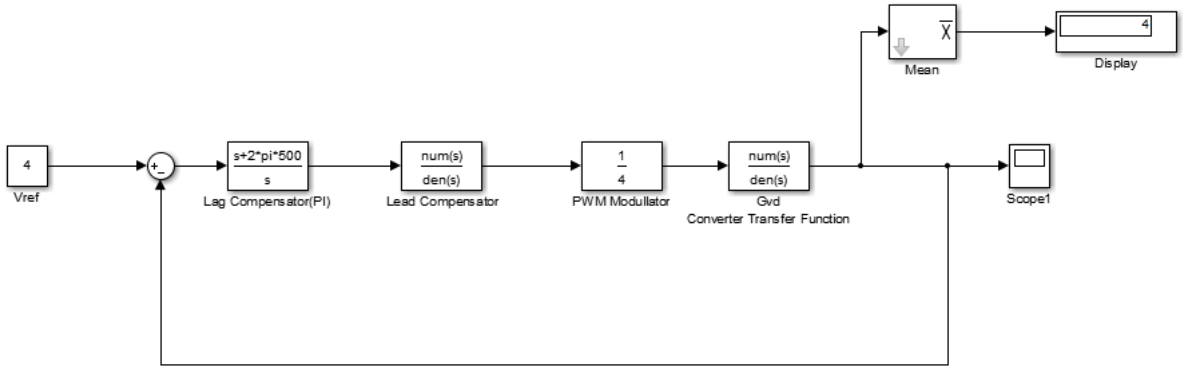

Fig 7: Simulink Transfer function based block diagram of compensated system

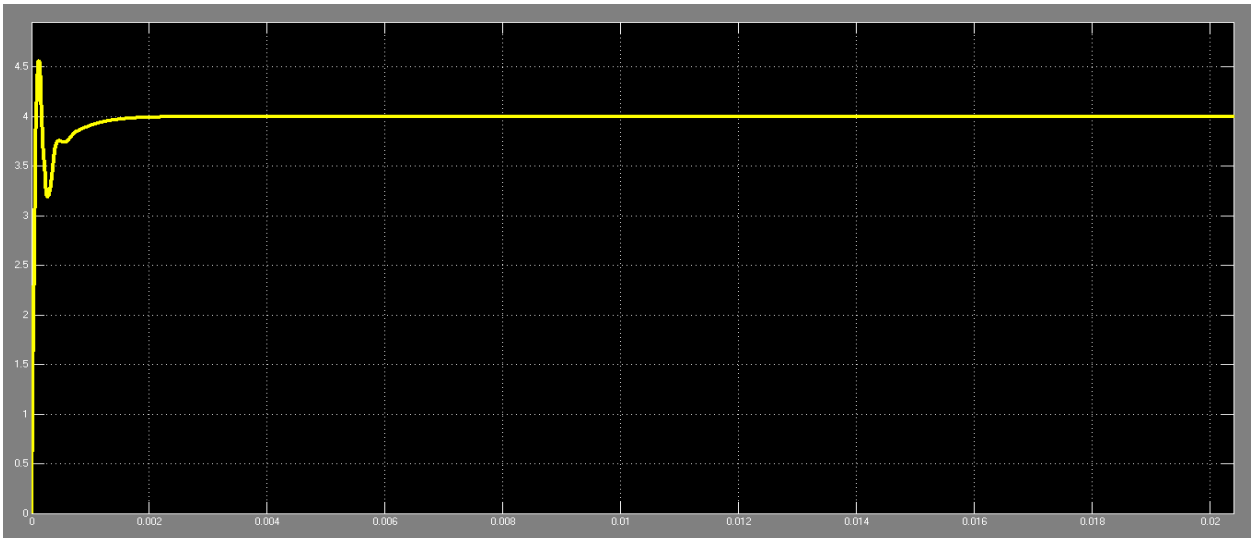

Fig 8: Output voltage vs time (both lead and lag compensators used)

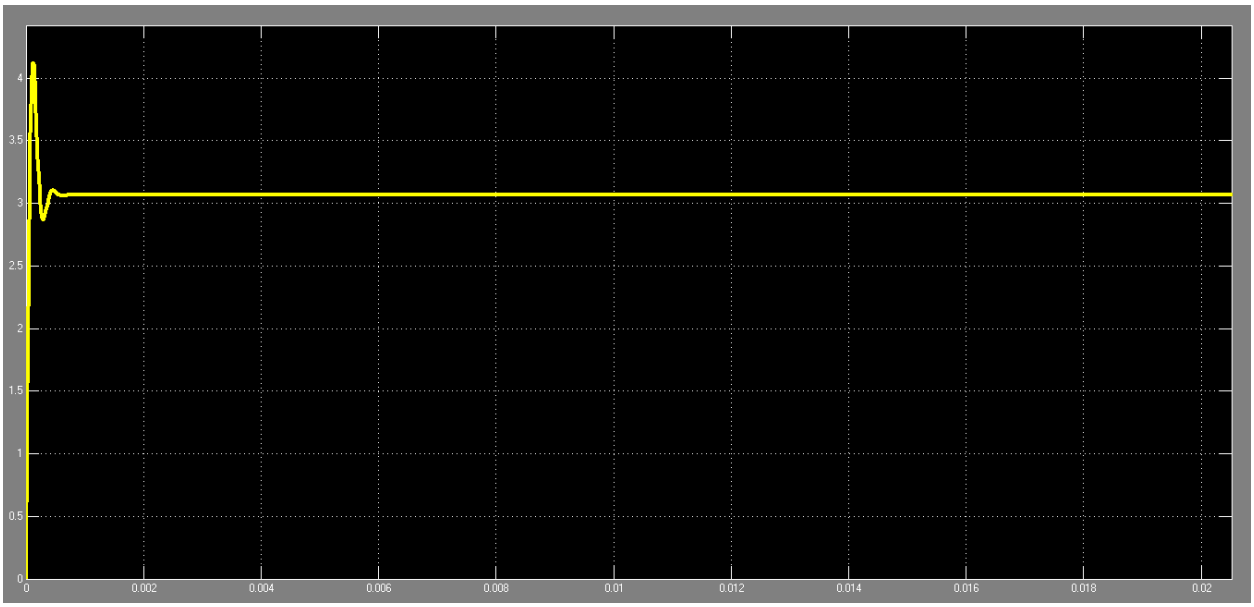

Fig 9: Output voltage vs time (with lag (PI) compensator removed)

Here we can see that when the lag compensator is not used the steady state error is very high, the required output is 4 V but here the output is little above 3 V. This shows the necessity of introducing a lag compensator in the loop.

Next we move on to see the circuit simulation in Simulink.

b. Circuit Simulation in Simulink

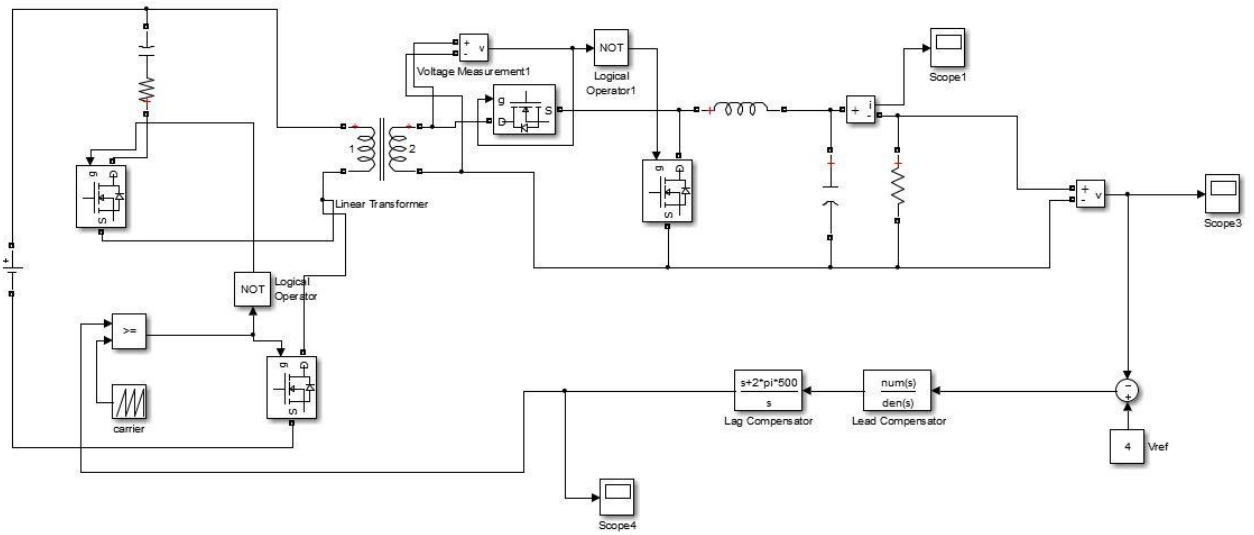

Fig 10: Closed loop Circuit schematic in Simulink Environment

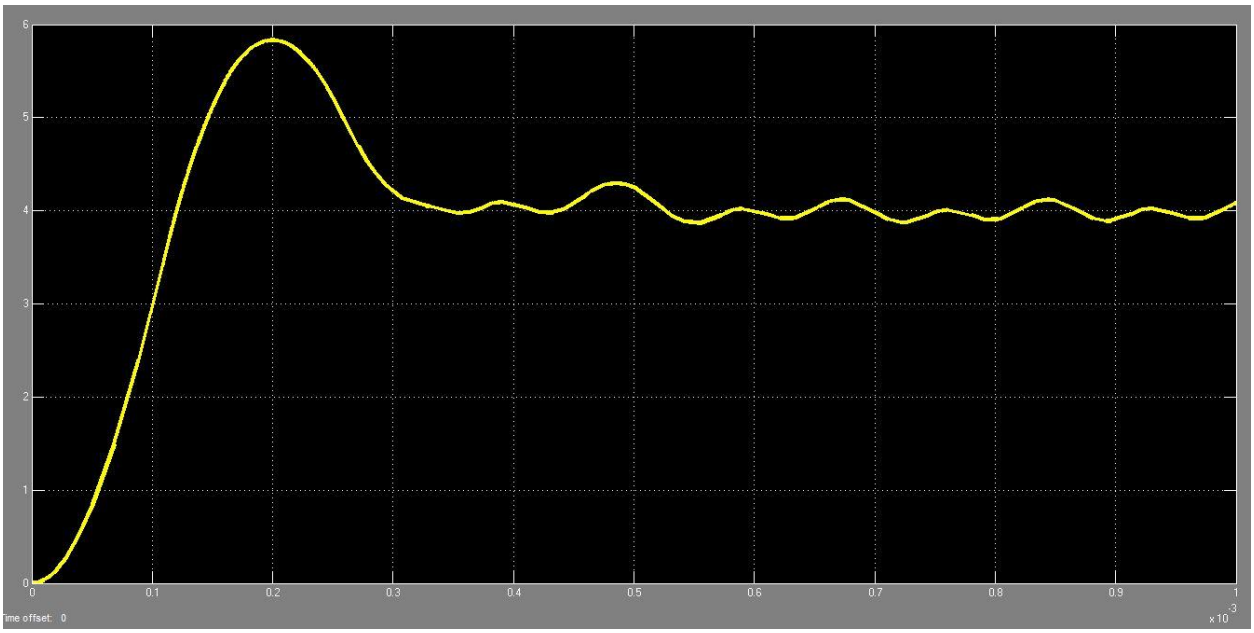

Fig 11: Voltage waveform of the compensated circuit

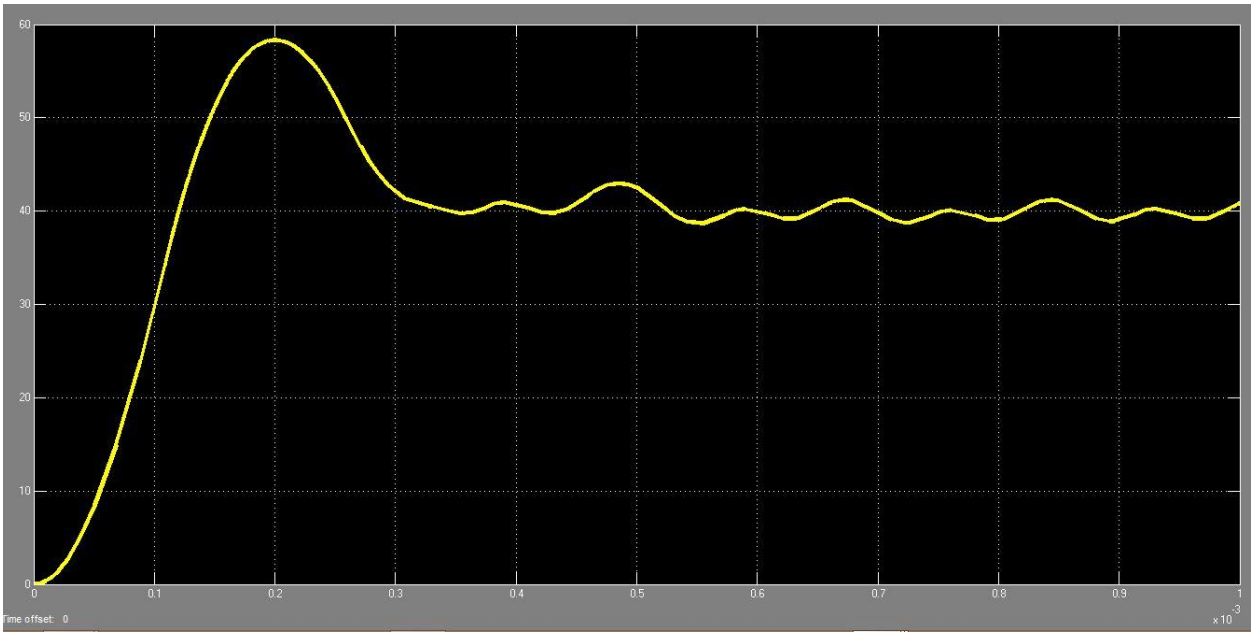

Fig 12: Current Waveform of compensated circuit

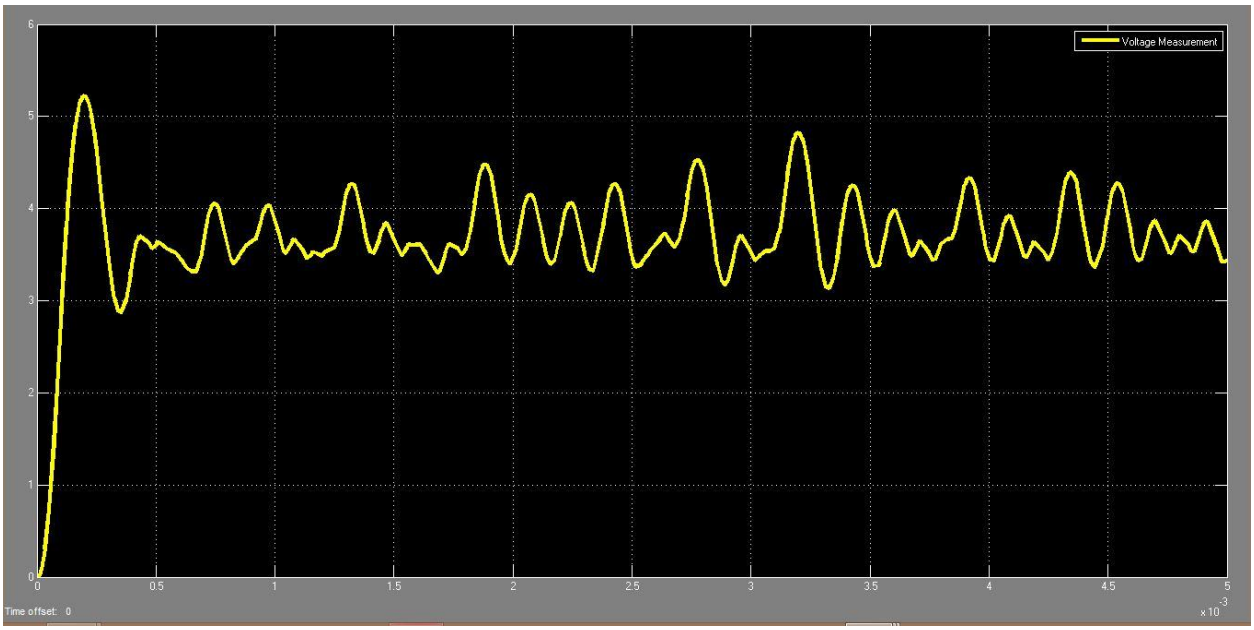

Fig 13: Voltage waveform of the circuit with only lead compensator

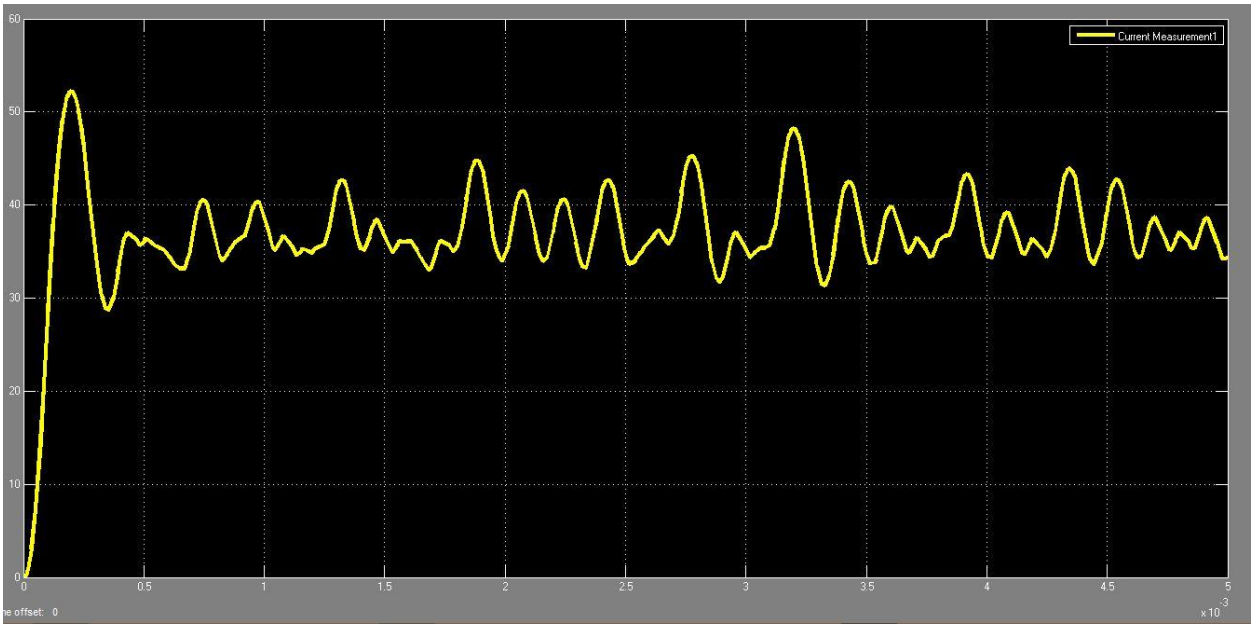

Fig 14: Current waveform of the circuit with only lead compensator

In the previous two figures we see that the voltage and current waveforms become oscillatory and also have greater steady state error. These graphs show the importance of introducing the lead compensator in the system.

Chapter 4

CONCLUSIONS AND FUTURE WORK

In this project, an attempt was made to study the functioning of the active clamp forward converter circuit. The most fascinating phenomena that I came across in this project was how transformers are used in DC devices with the aid of PWM switching. The graphs of the pulsating DC signals in the transformer primary and secondary were seen in the pSpice simulation. In literature the system analysis of low side clamp circuit is not available and one of the novelties of this thesis is the complete analysis of the low side clamp circuit by dividing each switching cycle into ten different modes. Following this a small signal modelling of the converter circuit was done. The small signal model helped obtaining a transfer function and this transfer function helped in developing a simple PID controller for the converter. The PID controller was simulated in SIMULINK. The effect of PI controller on achieving steady state stability was also examined.

The Active Clamped Forward Converter topology is still in the developmental stage and many researchers are bent on exploring this circuit topology. Simulink simulations don't take into account the effect of real world non idealities. So, in the future, pSpice simulations can be done to study the functionality of this circuit. Though this thesis has reported the open loop simulations in pSpice, it has failed to develop a closed loop design in this software owing to lack of the luxury of time. Besides doing a closed loop analysis in pSpice, the simulations must be verified by testing the circuit on hardware. In most literature authors have generally worked on the high side clamping circuit because in this type of clamping both the main switch and the auxiliary switch are N-MOSFETs making it easier to provide gating pulses but in low side, the main switch is N-MOSFET and the auxiliary switch is P-MOSFET thus making it bit difficult to provide switching pulses. So the Active clamp converter with low side clamping has a lot of potential for future research and a lot of its functionality seems still unexplored.

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